Preliminary Design Work on a DSN VLBI Correlator

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The DSN is in the process of fielding high-density digital instrumentation recorders for support of the Pioneer Venus 1978 Entry Experiment and other related tasks. It has long been obvious that these recorders would also serve well as the recording medium for VLBI experiments with relatively weak radio sources, provided that a suitable correlation processor for these tape recordings could be established. This article describes the overall design and current status of a VLBI correlator designed to mate with these tape recorders.

I. Introduction

The DSN is in the process of fielding high-density digital instrumentation recorders for support of the Pioneer Venus Entry Experiment (Ref. 1) and other related tasks. It has long been obvious that these recorders would also serve well as the recording medium for VLBI experiments with relatively weak radio sources, provided only that a suitable correlation processor for these tape recordings could be established. This article describes the overall design and current status of a VLBI correlator which we had planned to mate with these tape recorders. This design work began in mid 1976 and is terminating as of EO FY'77 with the transfer of Design Responsibility for the VLBI Correlator to DSN Implementation.

II. Overview of a VLBI Correlation Processor

The role of the VLBI correlation processor can best be understood by reference to Fig. 1, which shows the entirety of the VLBI instrumentation, exclusive of calibration tools. Acquisition of the VLBI data, a broadband noise signal from a

natural radio source, occurs in the Tracking Stations shown at the left of Fig. 1. Data from the two widely separated data acquisition sites are brought together at the correlation processor by shipment of the tape recordings, which can contain in excess of 10¹⁰ bits each.

There is a relative delay d between the arrival of the noise signal at the two tracking stations that depends upon the observing geometry: the relative position of the two stations on the Earth, the position of the radio source, and the position of the Earth at the instant of arrival. At each tracking station, the signal is filtered, translated in frequency by a local oscillator, sampled and quantized to one-bit (sign only) for recording. The principal function of the correlation processor is to perform cross-correlation detection of these sampled signals to estimate as precisely as possible the delay d, and the amplitude of the radio-source noise signal. The delay d must be known well enough a priori to be compensated for in the alignment of the recorded bit streams and in the doppler reference signal shown in Fig. 1. This can be accomplished either by providing precise polynomial predicts for each observation, or by allowing the correlation processor to compute from the observing geometry. In either case, the predicted delay must be computed to an accuracy which is compatible with the intended final system precision, and much more accurately than is needed to simply perform the correlation detection. Inaccuracies in the models used to predict d can be mostly eliminated by computing for the output interface the total estimated delay, instead of the offset from the model. Inaccuracies in computing the modeled delays directly become inaccuracies in results.

The summed bit-wise cross-products of the sampled data streams are an intermediate output from the correlation processor as shown. They are also a feasible interface that is comparable in complexity to the use of polynomials to predict the a priori delay. The signal detection operation is completed by estimating cross-correlation amplitude, delay, delay rate, phase and phase rate from the summed cross-products.

In designing any high precision, wide bandwidth VLBI System, it is often tacitly assumed that the wide bandwidth is achieved through the bandwidth synthesis technique (Ref. 2). Thus, a significant consideration in our correlator design was that it be capable of bandwidth synthesis operation with the 4 Mb sample rate of the Mark II recorders (Ref. 3). The DSN Instrumentation recorders could be easily partitioned into six such channels. If additional tracks are implemented, then eight 4-Mb channels can be extracted through relatively simple stream-partitioning electronics. We believe that the incremental cost of these additional tracks is low enough that they should be implemented when the tape recorders are configured for VLBI use. Our basic correlator design includes eight 8-Mb correlator channels, which would typically be run at the 4-Mb rates in bandwidth synthesis operation. Each correlator channel computes bit-wise cross products for an adjacent eight complex "lags." The channels can be concatenated to form a single 64-lag correlator for searching through a range of delays when the delay is only poorly known a priori. The channels can also be connected in tandem to provide a wideband single channel correlator.

III. Overview of Correlator Hardware

Figure 2 is a functional block diagram of the correlation processor hardware. Fundamental structure and parameter values in this design are based largely upon the recently completed Mark-II correlator at C.I.T. Some changes from the CIT design, such as including delay rate and phase acceleration terms, and extending the length of the accumulator and phase-reference registers, have been made to eliminate minor deficiencies seen in the earlier design (Ref. 4). We have also provided the capability to read the contents of the phase-reference generator registers into the computer to verify its operation, and enhance the accountability of its phase.

The tape recorders shown in Fig. 2 are the high density instrumentation recorders described by Kimball (Ref. 1). The tape control unit must adjust the relative position of the tapes during playback so that the data streams are approximately in time correspondence. The final alignment of data streams is done in the variable delay buffer between the tape recorders and the correlator proper. This buffer must be large enough to adapt the changes in delay needed to retain the proper alignment of data streams at the correlator to the dynamical capabilities of the tape recorders. The design-wise simplest system has the tapes completely aligned in time with all adjustments for observing geometry made in the variable delay buffers. In this case, however, the buffers are large, containing enough data to shift the delay by an Earth-radius or about 1.6×10^6 bits if tapes are played at 64 Mb.

The stream partitioning is a parallel-to-serial conversion into the 4-Mb channel bit streams from the parallel word of the tape recorder. It appears after the variable delay to allow the delay buffer to be a single entity. The variable delay could follow the stream partitioning, resulting in a more modular structure to the correlation processor, but at the cost of having eight identical variable delay buffers responding in concert to the delay adjustment commands.

The actual cross-correlation of the two data streams takes place in the correlation pre-scaler module. There, the bit stream from one channel on one tape is multiplied by quadrature "sine waves" from the phase reference generator. and by eight adjacent delayed copies of the bit stream from the corresponding channel on the other tape. The phase reference generator provides doppler compensation. The correlation prescaler also multiplies each of the data streams individually by quadrature "sine waves" to coherently detect the tones of the phase calibrator, which is necessary for accurate bandwidth synthesis VLBI. The low-order counter bits for the summation of cross-products are the "pre-scaler" part of correlation prescaler. Overflows from these short counters are transferred to the master accumulator. One correlation prescaler, and one phase reference generator share a physical module associated with one data channel.

The master accumulator is one physical module, which adds the overflows from up to eight prescaler units into a random access memory. Correlations are summed into only one half of this memory at a time, while completed sums can be transferred at leisure into the controlling computer.

The master timer contains a microprocessor which computes the phase and phase-rate data values for each of the phase reference generators from the phase, phase rate, and phase acceleration data provided by the controlling computer. It computes the delay, as a function of time, for the variable

delay buffer from the delay and delay rate data provided by the controlling computer. It contains the logical timing chains needed to relate "data time," as counted from the clock pulses from the tape recorders, to the event timing within the phase reference generators, and master accumulator.

The computer interface unit provides the controlling computer the capability to control the master timer and read the accumulated correlations. We also intend it to provide the capability to read the phase reference generator registers for diagnostic purposes. In addition, pathways would be provided to supply a data stream from the controlling computer into each of the correlation prescalers. This would provide a tool for test and diagnosis of the system operation. In addition, this path would allow real data recorded on computer-compatible tapes to be processed by this correlation processor, or perhaps on a subset machine that contained only one phase reference/correlation prescaler module.

The following sections present details of the VLBI correlator hardware.

IV. Lobe Rotator

The phase-reference generator, or the lobe rotator, is a device that supplies doppler sine and cosine information to the correlator. The sine-cosine outputs are two bit approximations to a sine wave. One of these two bits is used to control whether the signal from Station A is to be compared to the signal from Station B or to its complement. The second bit controls whether the correlated waveforms are to be counted or not. Figure 3 shows the composite waveforms of the sine and cosine.

The lobe rotator consists of four 32 bit registers, a 32 bit adder, a 32×8 ROM for converting the sine and cosine, and control circuitry. A block diagram is shown in Fig. 4. The four registers are called the A, B, $\Delta \Phi$, and Φ registers, with the adder connecting the $\Delta \Phi$ and Φ registers.

The ϕ register holds the value of the present phase, and is updated each clock pulse by the amount in the $\Delta \phi$ register via a 32 bit adder to be described in detail below. The 5 most significant bits of the ϕ register are used as the address of a 32 word ROM which contains the two-bit approximations to the sine and cosine.

The A and B registers are hold registers for the $\Delta \Phi$ register. Two hold registers were needed to handle the two different modes of controlling the Φ register. The first of these modes simply changes $\Delta \Phi$, which will result in a new rate of change for the contents of the Φ register. The second mode introduces a phase shift into the output phase and then changes $\Delta \Phi$ one

clock pulse later to produce a new slope for the phase information. This second mode requires the second hold register. When the B register is loaded with the phase shift value and the A register has the new $\Delta \Phi$, a command can be given to clock the B register into the $\Delta \Phi$ register and the A register into the B. One clock pulse later, the B register is again transferred into the $\Delta \Phi$ register to establish the new phase rate.

The A register is divided into 4 eight-bit byte sections. The first of these four sections is connected to a data bus that will be driven by the output of a microprocessor. When an A register clock is supplied from signals delivered by the microprocessor, the 8 bits from the data bus are clocked in the first section of the A register and each of the other three sections receives the 8 bits from the section to its left in shift register fashion. After 4 bytes have been loaded into the A register, a command may be sent to the lobe rotator by the microprocessor, to parallel transfer all 32 bits into the B register, in preparation for the transfer into the ϕ register as described above.

The adder used in the lobe rotator is of an unusual design necessitated by the requirement that the 32-bit sum be accomplished in 120 ns. Figure 5 shows a block diagram of the adder. For clarity, the inputs from the two registers are not shown. The technique used in the adder is to break the sum into four groups of 8 bits each. The carry into the least significant group of bits is known to be zero, and so a regular adder can be used. Each of the groups containing more significant bits are added twice, once with the carry set to zero and once with it set to one. The actual carry is computed in parallel and used to select the correct sum via a multiplexer. Adding each group of four bits twice does not increase the hardware chip count; since the carry output of an adder with a zero carry input is a term usually called Generate (G) in carry look-ahead schemes, while the output of an adder with the carry input set to one is a term usually called Propagate (P). Generate means that the group being added will generate a carry by itself, while Propagate means that the group being added will propagate an input carry to the next group above. The carry look-ahead equation is

$$C_n = G_{n-1} + P_{n-1} G_{n-2} + P_{n-2} P_{n-1} G_{n-3} + \cdots$$

where the subscripts n would refer to a group of eight bits. Figure 5 shows two SN74S64 used to compute the actual (inverted) carries \overline{C}_{15} and \overline{C}_{23} , which, in turn, are used to select the correct sum via the SN74LS157 multiplexer. The 32-bit sum through the adder, the carry computation and select takes 66-ns worst case, which allows ample time for register output delays and input setup times in the 120 ns time allotted.

V. Correlation Prescaler

The basic correlator design includes eight 8-Mb correlator channels each of which computes bit-wise cross products for eight adjacent complex "lags." In addition, each channel computes 7 other sums that are used to calibrate the system and in the computation of the final results. These signals are:

- (1) Total clock pulses minus tape bad signals
- (2) Total clock pulses minus tape bad or sine = 0
- (3) Total clock pulses minus tape bad or $\cos = 0$
- (4) Sin Ref \bigoplus A(n) but not tape bad
- (5) Sin Ref (B(n) but not tape bad
- (6) Cos Ref \bigoplus A(n) but not tape bad
- (7) Cos Ref \oplus B(n) but not tape bad

Each channel was built with these 23 correlation counters and one spare to make 24 per channel and 196 total in the system. The correlation prescaler counts the agreements between signal A(n), (the *n*th channel from tape recorder A and the signal B(n). It is assumed that each "channel" of the tape recorder also supplies a bad tape signal which is used to inhibit the correlation counter when the signal is known to be bad. Each counter in the prescaler consists of 8 bits, out of a total of 31 bits in the correlation accumulator.

The most significant bit from each of the 24 counter forms the output of the prescaler. These most significant bits from each counter are sampled every 15 μ s and stored in a shift register. Between the 15 μ s sampling times, this 24-bit shift register shifts the most significant bit of each counter to the master accumulator to be further processed.

The correlation prescaler also provides the gating for rearranging the available storage registers (lag-registers) in various ways. Figure 6 shows a block diagram of the eight bits of storage on two adjacent channels, channel n and channel n+1 where n is assumed to be even. Each of the four boxes shown in Fig. 6 is an SN74LS163 (a four bit shift register) which also can be parallel loaded depending upon the status of the S/\overline{L} signal. The chip is wired so that the lower three bits act as a shift register for either state of S/\overline{L} . This means that S/\overline{L} actually only controls which of two inputs to the shift register shall enter. The shifting input is shown vertically while the loading input is shown horizontally.

Under regular correlation conditions, all four shift registers are given the shift command and the input signal B(n) is delayed eight units of time necessary for the correlation.

Another desired configuration is to concatenate all the lags together. This mode is useful in initialization when the position of the correct lag is more uncertain than 8 positions. If the upper shift register in each channel (except the first) is signaled to load, the input to each register will be L(n-1), i.e. the output of the preceding channel. If the lower shift register is still in the shift mode, this accomplishes the desired arrangement.

One other mode of the S/\overline{L} signals is very useful. When the top two units shift (i.e., input B(n) and B(n+1)) and the bottom two load, (input B(n+1) and B(n) respectively), correlation can be a double sideband operation, i.e., where adjacent tracks on the tape are real and imaginary components of the signal. In this case, only 4 lags per channel are obtained. This same mode of operation is also useful when the adjacent tracks on the tape are even and odd samples of the same data, i.e., the data is coming in twice as fast as usual. In the mode described, it will be noticed that B(n) (the even bits of the sample) will be copied twice, once into the top register on the left and once into the lower 4-bit register on the right. A similar situation exists for the odd numbered signal bits. The A(N) signals, not shown on the diagram for clarity, are also assumed to be even and odd numbered bit stream from the other recorder. Thus, the even bits of B are correlated with the even bits of A on the top 4 bits at the left, the even bits of B correlated with the odd bits of A on the lower left, etc. The net result is to have 8 lags for half as many the original channels. Also, the correlation sum is broken into two parts and will have to be added together by the master computer.

VI. Master Accumulator

The master accumulator takes the eight streams of most significant bits from each correlator prescaler and uses this information to form the 23 most significant bits of the correlation sum.

The master accumulator is divided into three sections, an input section, an intermediate summing section and the final output accumulator stage. Each section has a major timing cycle of $15-5/8~\mu s$ during which the 24 parallel computations are made. The $15-5/8~\mu s$ major cycle time is divided from the 8-MHz clock rate at which the data enters the correlator prescaler. At this rate, the most significant bit of any prescaler counter can change only every $16~\mu s$. The $15-5/8~\mu s$ cycle time contains 24 minor timing cycles of $5/8~\mu s$ each for processing the information from the 24 prescaler counters and one extra cycle to allow one memory access for output.

The input section to the master accumulator contains a 24 word by 8 bit memory. Each word of this memory holds a copy of the MSB from the prescaler counter for each of the channels. One word of the memory is used for each of the 24

counters on the prescaler. The input for the master accumulator is the present value of this MSB which together with the previous value can be used to determine if an overflow of one of the counters occurred in the last major cycle. The output of this first section of the master accumulator is 8 bits each minor cycle, with a logic 1 for an overflow in each of the 8 positions. These overflow bits feed the intermediate summing section, which consists of eight 48 word by 4 bit memories, one for each of the eight channels. On each minor cycle of 5/8 us, a word is accessed from each memory, loaded into a 4 bit counter, and incremented if the overflow bit from the input section is set, and returned to memory. Only half of the 48 words are used during any major cycle, the other half holding the results from the previous correlation interval. This intermediate summation is done to further reduce the overflow rate from any counter. The prescaler had to be sampled every 16 μ s but an overflow from one of those counters could only occur every 32 µs. The overflows from this intermediate counter can occur at a maximum rate of 1 every 512 µs and so the most significant bit of this stage must be sampled more frequently than once every 256 µs. Actually, these bits are sampled every 125-130 us depending upon how many cycles are stolen for output. The eight most significant bits of each counter on the intermediate stage are sampled every eight or nine microseconds, and stored in an 8 bit shift register to be shifted to the output accumulator. The sampling is done in an 8-8-9 μ s pattern to get all 24 positions of the 8 channels from the intermediate stage sampled in 125 μ s. This time will be increased by $5/8 \mu s$ for each cycle stolen to output data from the previous correlation interval. Since one of these output cycles is constrained to occur only once every major cycle (15 μs) only 8 minor cycles or 5 μs at most will be added to the 125 µs figure above, to transfer all the overflows from the intermediate stage to the output accumulator.

The output accumulator stage of the master accumulator consists of two 196 word by 20 bit memories. The two memories have their outputs on a common buss and as before, one section holds the data from the previous correlation interval, while the other half of the memory is used for the present accumulation. During each minor cycle, the 20 bits are loaded into an up counter and incremented if the overflow bit from the intermediate stage is a one. An all-ones detector is included in the counter that inhibits further counting if the value is at a maximum. The 20 bits from the output stage and 3 bits from the intermediate stage are supplied as inputs to a 23-bit register that holds these bits for output. This output register is sent through a multiplexer to the host computer as three consecutive bytes.

Although the design of the master accumulator may seem overly complex, the hardware savings due to this design, as

compared to straight binary counters, makes it worth while. The master accumulator replaces 196 counters of 23 bits each, which if built with 4 bit binary counters would use 1,176 chips, not including any chips for output. The present master accumulator uses 95 chips including timing and output plus 3 extra chips on each prescaler for a total of 119 chips in an 8 channel system.

VII. Master Timer

The master timer is the unit that controls the overall signal flow in the correlator. This unit is responsible for supplying the $\Delta \phi$ information to all eight lobe rotators as well as calculating these values from the $\Delta\Delta\phi$ information determined by the geometry of the VLBI observation and supplied by the controlling computer. At least part of the master timer will utilize a flexible high-speed microprocessor, such as the Z80. The master timer will also have timing chains running at 8 MHz. These timers will be controlled by the microprocessor and are necessary to control transfers to the lobe rotators with an 8 MHz precision. The microprocessor in the master timer would do the 48-bit additions necessary to calculate the new $\Delta \Phi$ from the $\Delta \Delta \Phi$'s. The processor would also be responsible for controlling the time at which all 8 lobe rotators simultaneously receive the updated $\Delta \Phi$ s as directed by the control computer. The microprocessor would also be responsible for clearing the ϕ and $\Delta \phi$ registers of all lobe rotators at the start of a correlation interval. Starting the correlation after this would then be similar to changing $\Delta \Phi$.

As the correlation process continues, one data stream slips with respect to the other due to the rotation of the Earth. If no correction were made, the best lag at the highest correlation counter would drift out of the range of the 8 lags provided. For this reason, one data stream is moved periodically by one bit with respect to the other. With a sampling rate of 8 MHz, lags are separated in time by 120 ns, which corresponds roughly to a distance of 40 m at the speed of light. When the two stations move differentiately, so that one is about 40 m further from the star, a signal is given to the hardware to change the lag by one. A rough calculation of the minimum time for two stations on earth to move apart from a star by 40 m gives about 100 ms. The master timer would handle the details of the timing shift. If single side band sampling is used, there is an approximate 90 deg shift in the ϕ accompanying such a change of lag. In this case, the microprocessor would load both registers of the lobe rotator and give a command to change the phase followed by a change in $\Delta \phi$. In double side band sampling there is no 90 deg phase shift when the lags are changed.

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VIII. Tape Recorder Interface

The tape recorder interface has two main sections: the tape control unit and the buffer memory and its controls. The tape control unit supplies signals to the tape recorder to act as a vernier on its speed. This correction is needed to establish time correspondence between data samples on the two tape recorders.

The tape control unit also must read and interpret the time information on the tapes so as to be able to approximately align the tapes before the run starts.

The buffer memory is needed to provide a variable delay between the tape recorders and the correlator accumulators. The buffer must be large enough to accommodate the doppler shift of the data streams over, for example, a 20-min run, which is 12,000 bits per channel at a doppler slippage rate of 10 bits/s.

The conceptually simplest interface between the tape recorder and the correlator is to have a buffer large enough to accommodate 25 ms worth of data, which corresponds to the maximum signal path delay between any two stations. This buffer would be about 1.6×10^6 bits if the tapes are played at 64 Mb. This may turn out to be the best solution, however, since only 100 of the recently introduced 16K bit memory integrated circuits would be needed. If such a large memory were used, it would be necessary to switch its input between the two tape recorders as either recorder may lead or lag the other as various signal sources are scanned.

IX. Summary and Status

This article describes the initial design work on a high-speed digital VLBI correlator that could mate with the high-density digital instrumentation recorders. This correlator has 8 complex channels with 8 lags in each.

These channels are capable of being rearranged into either 4, 2 or 1 channels with a corresponding number of lags equal to 16, 32, or 64, respectively. Each of the 8 channels has a lobe rotator or phase reference generator to control the sine and cosine correlations. These lobe rotators have 32-bit arithmetic units to compute the phase from the phase rate information. The most significant 5 bits of the phase are used to compute the 3 level sine and cosine approximations from a ROM. Each accumulator on each of the 196 lags in the correlator has 31 bits. The most significant 23 bits of these registers are double buffered to allow their transfer to the controlling computer.

At this time, the lobe rotator and correlation prescaler units have been designed, built, and debugged. It has been confirmed that the 32-bit arithmetic unit works at its 8-Mhz design limit. The master accumulator has been designed and is under construction. Both of these units have been configured on a DSN standard integrated circuit packaging panel. The lobe rotator-prescaler module occupies one panel while the master accumulator is slightly less.

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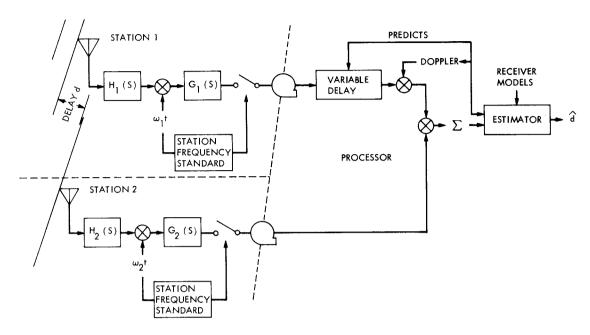


Fig. 1. VLBI instrument (simplified)

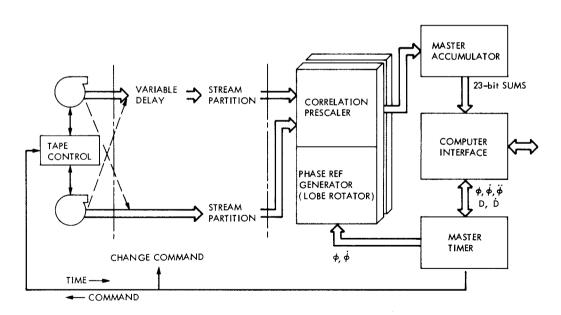


Fig. 2. VLBI correlation processor

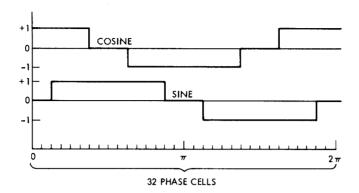


Fig. 3. Sine and cosine approximations

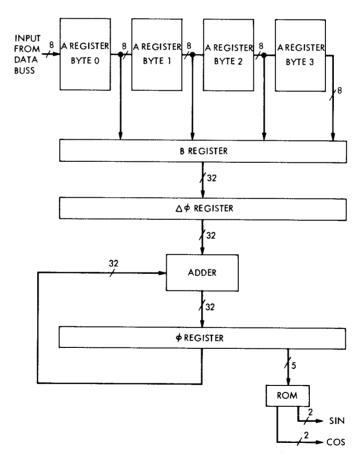
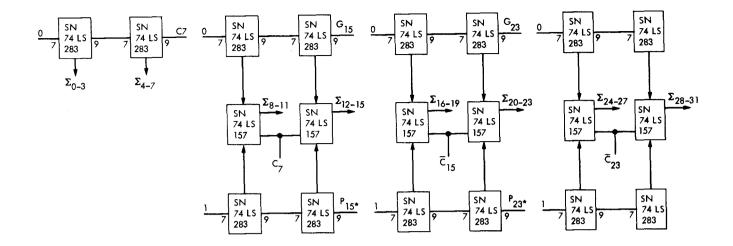


Fig. 4. Lobe rotator block diagram



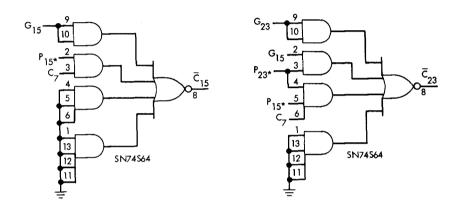


Fig. 5. Adder block diagram

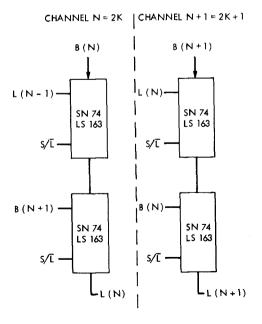


Fig. 6. Lag rearrangement